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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 33/00	A1	(11) International Publication Number: WO 98/37586
		(43) International Publication Date: 27 August 1998 (27.08.98)

(21) International Application Number: PCT/US98/03146

(22) International Filing Date: 18 February 1998 (18.02.98)

(30) Priority Data:
9/37705 21 February 1997 (21.02.97) JP

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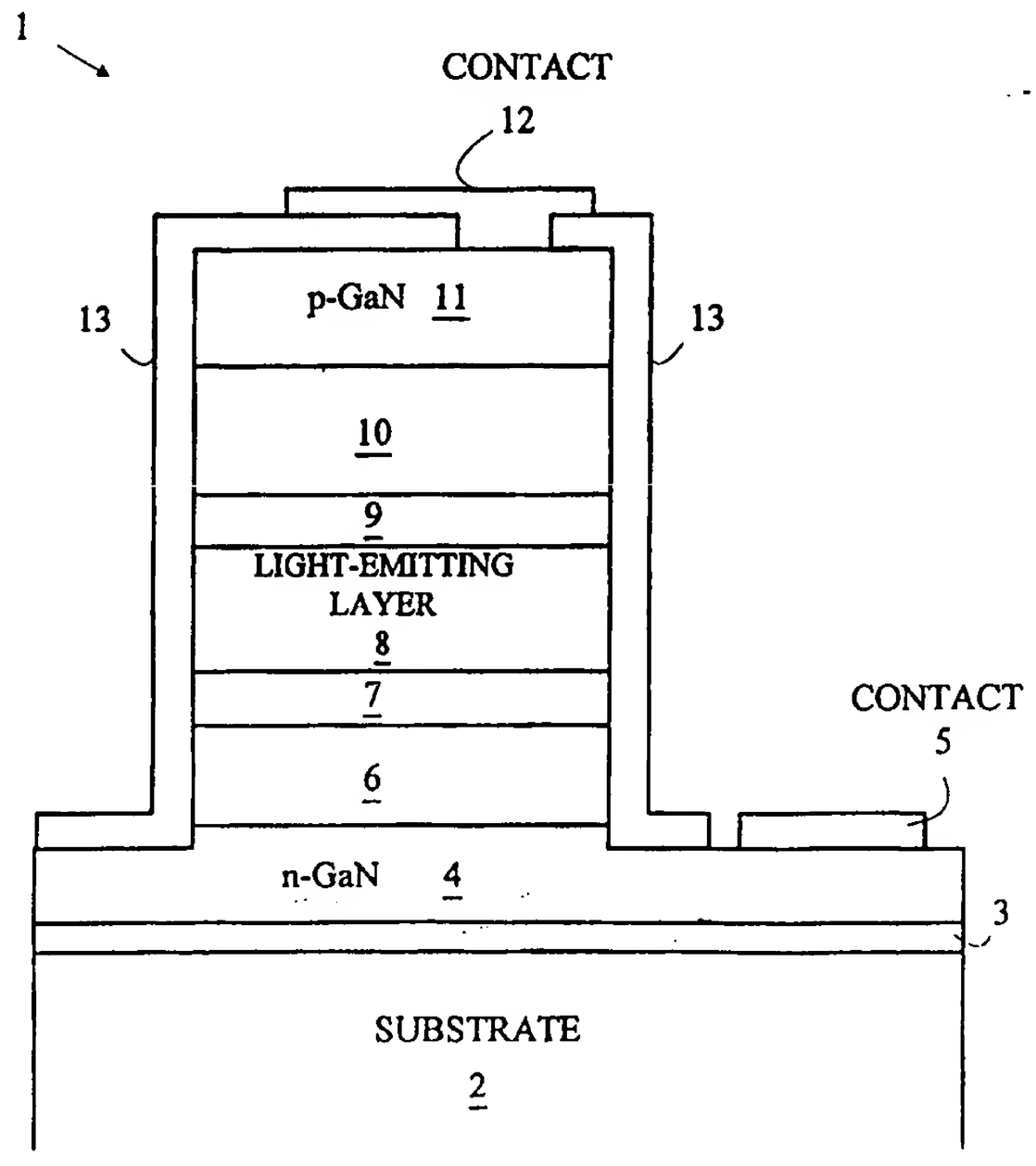
(81) Designated States: US, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: METHOD FOR FABRICATING LOW-RESISTANCE CONTACTS ON NITRIDE SEMICONDUCTOR DEVICES

(57) Abstract

A method for fabricating an electrical contact (12) on a surface (11) of a semiconductor comprising a group III element and nitrogen. The contact (12) is formed by depositing a metallic layer on the semiconductor surface and then annealing the layer at a tempeature greater than 400 °C for at least 4 hours. The method can be used to construct a Au/Ni contact on GaN semiconductor surface with substantially less resistivity than that obtained by conventional methods.



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METHOD FOR FABRICATING LOW-RESISTANCE CONTACTS ON NITRIDE SEMICONDUCTOR DEVICES

Field of the Invention

The present invention relates to methods for fabricating electrical contacts on semiconductor devices, and more particularly, to a method for fabricating an electrical contact with reduced contact resistance on group III-nitride semiconductor surfaces.

Background of the Invention

In the following discussion a III-N semiconductor is a semiconductor having a Group III element and nitrogen. III-N semiconductors such as GaN are useful in fabricating light emitting elements that emit in the blue and violet regions of the optical spectrum. These elements include light emitting diodes and laser diodes. In addition, III-N semiconductors can be used to construct metal semiconductor field-effect transistors (MESFETs).

In particular, laser diodes that use semiconductor material based on GaN that emit in the blue and violet regions of the spectrum hold the promise of substantially improving the amount of information that can be stored on an optical disk. However, to provide this improvement, the laser diode must operate in an essentially continuous mode while maintaining a lifetime consistent with a consumer product. Prior art GaN based laser diodes do not satisfy these constraints. In addition, prior art GaN-based laser diodes require high driving voltages and have low electrical efficiency.

Light emitting elements based on III-N semiconductors are typically fabricated by creating a p-n diode structure having a light generating region between the p-type and n-type layers. The diode is constructed from layers of III-N semiconducting materials. After the appropriate layers are grown, electrodes are formed on the p-type and n-type layers to provide the electrical connections for driving the light-emitting element.

The problems discussed above with III-N laser diodes are primarily due to the large contact resistance between the metal that becomes the electrode and the GaN material. This contact resistance is particularly high at the p-type electrode. For example, the contact resistivity between the metal electrode and the p-GaN layer of a typical device provided with Au/Ni electrodes is about 2×10^{-1} Ωcm^2. If the electrode contact area is 300 μm x 300μm, the contact resistance is above 200 Ω. At a drive current of 0.1A, more than 2 watts of power are consumed by the contact. The high contact resistance requires a larger driving voltage to overcome. In addition, the power dissipated in the contact generates a significant amount of heat. The heat prevents the devices from running in a continuous mode at the light output levels needed to read and/or write optical disks. In addition, the heat shortens the lifetime of the devices. Accordingly, a significant improvement in III-N laser diodes would be obtained if this contact resistance could be reduced.

Broadly, it is the object of the present invention to provide an improved method for constructing an electrical contact on III-N semiconductors.

It is a further object of the present invention to provide a method for constructing an electrical contact on III-N semiconductors with lower contact resistance.

These and other objects of the present invention will become apparent to those skilled in the art from the following detailed description of the invention and the accompanying drawings.

Summary of the Invention

The present invention is a method for fabricating an electrical contact on a surface of a semiconductor comprising a group III element and nitrogen. The contact is formed by depositing a metallic layer on the semiconductor surface and then annealing the layer at a temperature greater than 400 °C for at least 4 hours. The method can be used to construct a Au/Ni contact on GaN semiconductor surface with substantially less resistivity than that obtained by conventional methods.

Brief Description of the Drawings

Figure 1 is a cross-sectional view of a typical edge-emitting laser diode constructed from III-N semiconductor layers.

Detailed Description of the Invention

The present invention may be more easily understood with reference to a specific III-N light-emitting device. Refer now to Figure 1, which is a cross-sectional view of a III-N vertical cavity surface emitting laser 1. The laser is formed by depositing by depositing a number of layers on a sapphire substrate 2 and then etching back the layers to provide contacts to the n-type and p-type layers. The layers shown in the figure are a GaN buffer layer 3, an n-type GaN contact layer 4, an n-type A1GaN cladding layer 6, an n-type GaN optical waveguide layer 7, an InGaN multi-quantum well layer 8 for generating light, a p-type GaN optical waveguide layer 9, a p-type A1GaN cladding layer 10, and a p-type GaN contact layer 11. The n-type electrode 5 and the p-type electrode 12 are formed on the n-type GaN contact layer 4 and the p-type GaN contact layer 11, respectively. A SiO2 layer 13 covers the outer surface of the etched area. The construction of these layers and the etching processes used to provide access to the contact layers are conventional in the art, and hence, will not be discussed in detail here.

The conventional method for fabricating the metal contacts involves depositing a metal, such as gold (Au), platinum (Pt), nickel (Ni), or iridium (Ir) on the semiconductor, and then annealing the device at a high temperature for a relatively short time, typically, 1 to 2 minutes. A metal-semiconductor alloy forms at the interface of the semiconductor and deposited metal layer, and a stable ohmic contact is obtained. Unfortunately, the contact resistance obtained by this method is too high.

The present invention is based on the observation that the contact resistance decreases with annealing time. If very long annealing times are utilized, a reduction in the contact resistance of more than a factor of 30 has been observed. In the preferred embodiment of the present invention, GaN is used as the nitride semiconductor, and a Ni/Au electrode is utilized

for the p-GaN contact. The metals are deposited on the outermost p-type GaN layer utilizing vacuum deposition techniques based on conventional electron beam heating of an appropriate target. For example, a Ni layer is deposited on the GaN layer to a thickness of approximately 1.4 nm. Then, a Au layer is deposited to a thickness of approximately 200 nm on the Ni layer. The device is then annealed for at least 4 hours at a temperature between 400-600° C, typically 500° C. In the preferred embodiment of the present invention, the annealing operation is carried out at 500 ° C in a nitrogen atmosphere.

The resistivity of the contact is found to decrease monotonically with annealing time for annealing times between 4 and 16 hours. For example, a device having a contact as described above was found to have a contact resistivity of 6×10^{-2} Ωcm^2 before annealing. After annealing for 4 hours, the resistivity decreased to 1.3×10^{-2} Ωcm^2. After annealing for 9 hours, the resistivity decreased to 6.9×10^{-3} Ωcm^2. After 16 hours of annealing, the resistivity decreased to 1.6×10^{-3} Ωcm^2. This represents an approximately 35-fold decrease in the resistivity of the contact. It should be noted that the resistivity begins to increase again if the annealing time is greater than 16 hours. The decrease in the contact resistance with annealing time is believed to result from the diffusion of the Ni into GaN.

While the above example has utilized a specific III-N semiconductor and electrode structure, the teachings of the present invention can be applied to other semiconductors and electrode structures. In addition, the present invention may be applied to other devices than light emitting diodes.

Various modifications to the present invention will become apparent to those skilled in the art from the foregoing description and accompanying drawings. Accordingly, the present invention is to be limited solely by the scope of the following claims.

WHAT IS CLAIMED IS:

1. A method for fabricating an electrical contact[12] on a surface of a semiconductor[11] comprising a group III element and nitrogen, said method comprising the steps of: depositing a metallic layer on said semiconductor surface; and annealing said layer at a temperature greater than 400 °C for at least 4 hours.

2. The method of claim 1 wherein said semiconductor surface comprises GaN.

3. The method of claim 1 wherein said metallic layer comprises an element chosen from the group consisting of Au, Pt, Ni, and Ir.

4. The method of claim 1 wherein said metallic layer comprises a layer of Ni adjacent to said semiconductor surface and a layer of Au deposited on said layer of Ni.

5. In a circuit[1] having an electrical contact[12] comprising a metallic layer in contact with a p-type semiconductor layer[11] comprising a Group III element and nitrogen, the improvement comprising providing a metallic diffusion region in said semiconductor layer, said diffusion region having metal diffused therein and being in contact with said metallic layer, the concentration of metal in said diffused region being sufficient to lower the resistance of said electrical contact relative to the resistance of said electrical contact in the absence of said diffusion region.

6. The circuit[1] of Claim 5 wherein said p-type semiconductor layer[11] comprises GaN.

7. The circuit[1] of Claim 5 wherein said metal diffused into said semiconductor layer[11] comprises Ni.

8. The circuit[1] of Claim 5 wherein said metallic layer comprises an element chosen from the group consisting of Au, Pt, Ni, and Ir.

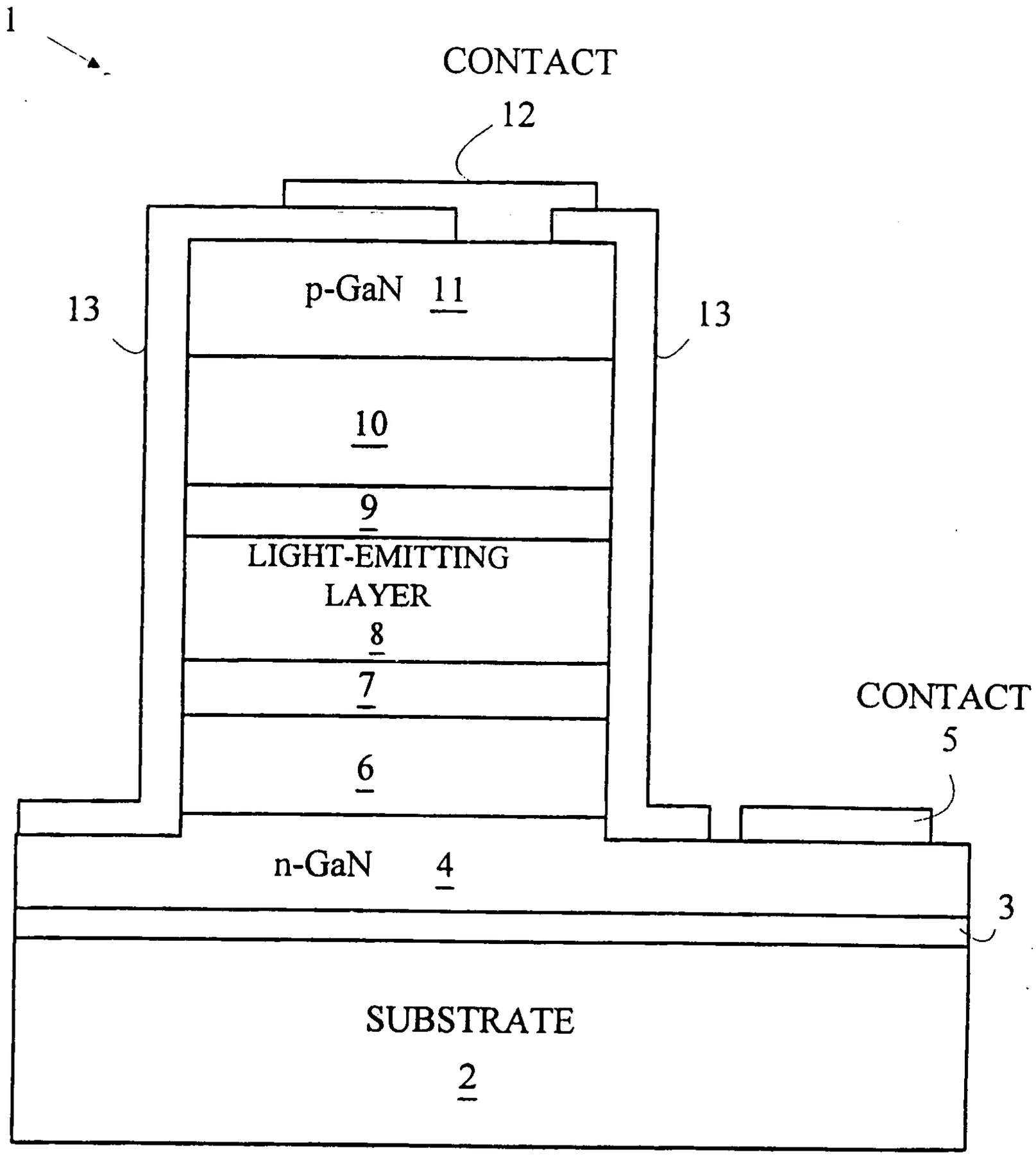
1
CONTACT
12
13
p-GaN 11
13
10
9
LIGHT-EMITTING
LAYER
8
7
6
CONTACT
5
n-GaN 4
3
SUBSTRATE
2

FIGURE 1

INTERNATIONAL SEARCH REPORT

Ir ational Application No
PCT/US 98/03146

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L33/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 622 858 A (NICHIA KAGAKU KOGYO KK) 2 November 1994 see page 6, line 26-47	5-8
A	---	1-4,9
A	ISHIKAWA H ET AL: "EFFECTS OF SURFACE TREATMENT AND METAL WORK FUNCTIONS ON ELECTRICALPROPERTIES AT P-GAN/METAL INTERFACES" JOURNAL OF APPLIED PHYSICS, vol. 81, no. 3, 1 February 1997, pages 1315-1322, XP000659459 see page 1318, paragraph 3	1-9

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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13 May 1998	22/05/1998
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INTERNATIONAL SEARCH REPORT

Information on patent family members

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